ABSTRACT OF THE DISCLOSURE

The present invention relates to an integrated circuit comprising a central processing unit clocked by a clock signal, a main oscillator circuit supplying a first clock signal and a peripheral circuit supplying a periodic wake up signal, the central processing unit comprising a first operating mode at full power, in which the first clock signal is applied to the central processing unit, and an active halt mode in which the main oscillator circuit and the central processing unit are deactivated, the central processing unit being awakened by the periodic wake-up signal. According to the present invention, the integrated circuit comprises a secondary oscillator circuit for supplying a second clock signal of lower frequency than the first clock signal and a circuit for managing clock signals arranged for, upon the wake-up of the central processing unit at the end of the active halt mode, waking up the secondary oscillator circuit and applying the second clock signal to the central processing unit so as to clock the central processing unit to the lower frequency of the second clock signal and thus obtain a second operating mode with reduced current consumption relative to the first operating mode.